WHAT IS CLAIMED IS:

1. An electrostatic discharge protection device, comprising:

a semiconductor substrate;

an isolation structure formed inside the semiconductor substrate;

a dielectric layer disposed over the semiconductor substrate and being in contact with the isolation structure; and

a layer of silicon, formed over the dielectric layer, including a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first p-type portion and the first n-type portion, a second n-type portion, a third p-type portion, a third n-type portion contiguous with the third p-type portion, and a fourth p-type portion contiguous with the third p-type portion and the third n-type portion, wherein at least one of the first p-type portion, second p-type portion, third p-type portion, fourth p-type portion, first n-type portion, second n-type portion, and third n-type portion overlaps the isolation structure to provide electrostatic discharge protection.

2. The device as claimed in claim 1, wherein the second n-type portion is contiguous with the second p-type portion.

3. The device as claimed in claim 1, wherein the third p-type portion is contiguous with the second n-type portion.

4. The device as claimed in claim 1, wherein the layer of silicon further comprises a first buffer portion disposed between the second p-type portion and second n-type portion.

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5. The device as claimed in claim 4, wherein the first buffer portion of the layer of silicon is doped with an n-type impurity having a doped concentration lower than one of the first n-type portion, second n-type portion, or third n-type portion.

6. The device as claimed in claim 4, wherein the first buffer portion of the layer of silicon is doped with a p-type impurity having a doped concentration lower than one of the first p-type portion, second p-type portion, third p-type portion, or fourth p-type portion.

7. The device as claimed in claim 4, wherein the first buffer portion of the layer of silicon is undoped.

8. The device as claimed in claim 1, wherein the layer of silicon further comprises a second buffer portion disposed between the second n-type portion and third p-type portion.

9. The device as claimed in claim 8, wherein the second buffer portion of the layer of silicon is doped with an n-type impurity having a doped concentration lower than one of the first n-type portion, second n-type portion, or third n-type portion.

10. The device as claimed in claim 8, wherein the second buffer portion of the layer of silicon is doped with a p-type impurity having a doped concentration lower than one of the first p-type portion, second p-type portion, third p-type portion, or fourth p-type portion.

11. The device as claimed in claim 8, wherein the second buffer portion of the layer of silicon is undoped.

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12. The device as claimed in claim 1, wherein all of the first p-type portion, second p-type portion, third p-type portion, fourth p-type portion, first n-type portion, second n-type portion, and third n-type portion overlap the isolation structure to provide electrostatic discharge protection.

13. The device as claimed in claim 1, wherein the layer of silicon is comprised of polysilicon.

14. An integrated circuit, comprising:

a first terminal;

a second terminal; and

an electrostatic discharge device coupled between the first terminal and the second terminal, comprising

a semiconductor substrate;

an isolation structure formed inside the semiconductor substrate;

a dielectric layer disposed over the semiconductor substrate and being in contact with the isolation structure; and

a layer of silicon, formed over the dielectric layer, including a first p-type portion, a first n-type portion contiguous with the first p-type portion, a second p-type portion contiguous with the first p-type portion and the first n-type portion, a second n-type portion, a third p-type portion, a third n-type portion contiguous with the third p-type portion, and a fourth p-type portion contiguous with the third p-type portion and the third n-type portion,

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wherein the first p-type portion, second p-type portion, third p-type portion, fourth p-type portion, first n-type portion, second n-type portion, and third n-type portion overlap the isolation structure, and

wherein the first p-type portion and first n-type portion are coupled to the first terminal, and the fourth p-type portion and third n-type portion are coupled to the second terminal.

15. The integrated circuit as claimed in claim 14, wherein the first terminal is coupled to a voltage source and the second terminal is coupled to a signal pad.

16. The integrated circuit as claimed in claim 14, wherein the first terminal is coupled to a VDD source and the second terminal is coupled to a VSS source.

17. The integrated circuit as claimed in claim 14, wherein the first terminal is coupled to a first signal pad and the second terminal is coupled to a second signal pad.

18. The integrated circuit as claimed in claim 14, wherein the layer of silicon further comprises a first buffer portion disposed between the second p-type portion and second n-type portion.

19. The integrated circuit as claimed in claim 14, wherein the layer of silicon further comprises a second buffer portion disposed between the second n-type portion and third p-type portion.

20. A method for protecting a complementary metal-oxide semiconductor device from electrostatic discharge, comprising:

providing a bi-directional silicon controlled rectifier in the complementary metal-oxide semiconductor circuit;

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isolating the bi-directional silicon controlled rectifier from a substrate of the complementary metal-oxide semiconductor circuit;

providing a signal pad coupled to the bi-directional silicon controlled rectifier for receiving an electrostatic discharge; and

protecting the device from the electrostatic discharge with the bi-directional silicon controlled rectifier.

21. The method as claimed in claim 20, wherein the electrostatic discharge is a positive discharge.

22. The method as claimed in claim 20, wherein the electrostatic discharge is a negative discharge.

23. The method as claimed in claim 20, wherein the step of isolating the bi-directional silicon controlled rectifier from a substrate of the complementary metal-oxide semiconductor circuit includes a step of providing an insulator layer between the substrate and the bi-directional silicon controlled rectifier.

24. The method as claimed in claim 23, further comprising a step of forming the bi-directional silicon controlled rectifier in a layer of silicon.

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